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Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

00204131.7

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

I.L.C. HATTEN-HECKMAN

DEN HAAG, DEN
THE HAGUE, 01/06/01
LA HAYE, LE

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Sheet 2 of the certificate
Page 2 de l'attestation

Anmeldung Nr.:
Application no.:
Demande n°: 00204131.7

Anmeldetag:
Date of filing:
Date de dépôt: 21/11/00

Anmelder:
Applicant(s):
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Bezeichnung der Erfindung:
Title of the invention:
Titre de l'invention:
Method of forming a semiconductor structure

In Anspruch genommene Priorität(en) / Priority(ies) claimed / Priorité(s) revendiquée(s)

Staat: State: Pays:	Tag: Date: Date:	Aktenzeichen: File no. Numéro de dépôt:

Internationale Patentklassifikation:
International Patent classification:
Classification internationale des brevets:
/

Am Anmeldetag benannte Vertragstaaten:
Contracting states designated at date of filing: AT/BE/CH/CY/DE/DK/ES/FI/FR/GB/GR/IE/IT/LI/LU/MC/NL/PT/SE/TR
Etats contractants désignés lors du depôt:

Bemerkungen:
Remarks:
Remarques:

Method of forming a semiconductor structure

The present invention relates to a method of forming a semiconductor structure comprising a substrate having a patterned Oxide-Nitride-Oxide insulating layer provided over a portion of the substrate.

An insulating layer in the form of Oxide-Nitride-Oxide (ONO) sub-layers is commonly employed as an insulting layer between a floating gate and a control gate of a non-volatile memory cell.

Such non-volatile memory cells are commonly integrated onto a semiconductor substrate adjacent to a peripheral structure such as a peripheral transistor. In order to simplify the fabrication process, the layer of, for example, polysilicon serving to form the control gate of the non-volatile memory cell can also be used as part of the peripheral transistor structure, such as providing the gate thereof.

The above-mentioned fabrication technique is one example of a process where an ONO insulating layer has to be selectively removed from regions of the substrate so as to allow for the required formation of a peripheral structure.

Standard prior-art processes have employed the provision of a patterned photoresist on the ONO insulating layer so as to allow for the selective etching of the ONO layer and to thereby provide for the formation of the appropriate peripheral structure.

However, disadvantages arise since, once the photoresist has performed its function, it is stripped from the structure and this stripping process serves to remove or at least damage the top oxide layer of the ONO insulating layer. Such problems are accentuated in situations where the top oxide layer of the ONO insulating layer is relatively thin and/or formed through deposition. The attack on this upper oxide portion of the ONO insulating layer therefore represents a particularly problematic feature.

US-A-6004847 discloses a process which serves to limit the above-mentioned problem in that, at the time of depositing a photoresist layer, the insulating layer comprises merely Nitride-Oxide sub-layers, i.e. an NO structure, and the upper nitride layer of which experiences much less damage than would the upper oxide sub-layer of an ONO structure during photoresist stripping. In this prior-art document, once the resist has been stripped, an

oxide layer is then deposited on the Nitride layer so as to form a complete ONO insulating layer structure.

The process and related structure disclosed in this prior-art document is nevertheless disadvantageously limited with regard to the quality and control of thickness of the layers that can be achieved in the final memory cell structure and peripheral structure.

The present invention therefore seeks to provide for a method of forming a semiconductor structure provided with a patterned ONO insulating layer and which exhibits advantages over such known methods and related structures.

According to one aspect of the present invention there is provided a method of forming a semiconductor structure as noted above and characterized by the steps of forming an insulating layer comprising an Oxide-Nitride-Silicon layered structure on the substrate, applying a photoresist to the silicon surface as part of a patterning process and stripping the photoresist once a required patterning step has been completed, and subsequently re-oxidizing the silicon layer of the remaining Oxide-Nitride-Silicon structure so as to form an ONO insulating layer structure.

The feature of claim 2 has the advantage of offering a good quality of oxidation of the silicon layer. The features of claims 3 and 4 relate to a particularly advantageous integrated structure benefiting from the present invention. The feature of claim 5 has the advantage that the re-oxidation of the silicon layer serves as a useful vehicle for forming a high voltage oxide layer in the peripheral structure.

The invention is described further hereinafter, by way of example only, with reference to the accompanying drawing in which;

Fig. 1 is a cross-sectional view of a non-volatile memory cell and integrated peripheral transistor structure to be formed in accordance with a method embodying the present invention;

Fig. 2 illustrates a cross-sectional view of an integrated semiconductor structure during the formation of the structure of Fig. 1;

Figs. 3A and B illustrate an enlarged view of part of the structure of Fig. 2 as deployed according to a method of the prior-art.

Figs. 4A and 4B illustrate a similarly enlarged view but employing a structure in accordance with an embodiment of the present invention.

Turning first to Fig. 1 there is illustrated a cross-sectional view of an integrated semiconductor structure 10 comprising a non-volatile memory cell 12 and an associated peripheral transistor structure 14.

The memory cell 12 and peripheral transistor 14 share a common substrate 16 while the memory cell 12 is formed, in ascending order as illustrated in the drawing, by a gate oxide layer 18, a floating gate polysilicon layer 20, an ONO insulating layer 22 and a polysilicon control gate 24. It is only the basic features of the peripheral transistor structure 14 that are illustrated in Fig. 1 and, again in ascending order, these comprise a gate oxide 26 formed from a continuation of the oxide layer 18 of the memory cell 12 and also a polysilicon gate layer 28 which comprises an extension of the polysilicon control gate 24 of the memory cell 12. In order to provide for the formation of the peripheral structure such as the peripheral transistor 14 illustrated in Fig. 1, the ONO insulating layer 22 which initially extends laterally over the majority of the integrated structure illustrated in Fig. 1 needs to be patterned i.e. removed from the regions of the substrate 16 where the peripheral transistor 14 is to be formed.

Such patterning is achieved by means of the provision of a photoresist 30 illustrated in Fig. 2. The photoresist layer 30 is first formed over the ONO layer 22 and then a photolithographic process serves to pattern the photoresist 30 so as to allow for a subsequent etching of the ONO layer 22 where no photoresist is present. Once the ONO layer 22 is effectively patterned by such etching, it eventually becomes necessary to strip the photoresist from the upper surface of the ONO layer 22. The illustration provided by Fig. 2 indicates the stage at which etching of the ONO insulating layer 22 has been achieved and just prior to stripping of the photoresist layer 30 from the ONO insulating layer 22.

It is at the time of stripping the photoresist layer 30 from the ONO insulating layer 22 that damage to the upper oxide sub-layer of the ONO structure occurs.

This particular aspect is illustrated further with regard to Fig. 3A and 3B.

Fig. 3A is an enlarged view of a portion of the ONO insulating structure 22 of Fig. 2 and in which a portion of the ONO insulating layer 22 having a portion of photoresist 30 thereon is illustrated in enlarged detail. As will be appreciated, the resist layer 30 actually contacts the upper oxide sub-layer 36 of the ONO insulating layer 22 and, at the time of stripping, serves to remove, and generally damage, the upper oxide sub-layer 36 as illustrated with reference to Fig. 3B in which the same portion of the ONO insulating structure 22 after removal of the photoresist 30 is shown.

According to an embodiment of the present invention rather than immediately forming the insulating layer as an ONO structure, an insulating layered structure comprising, again in ascending order, sub-layer of oxide 38, nitride 40 and silicon 42, is provided such that the photoresist 30 is then deposited on the surface of the silicon sub-layer 42. As illustrated in Fig. 4A there is then no exposed oxide to be attacked during the stripping of the photoresist. The upper silicon sub-layer 42 proves much more resistive to such detrimental attack such that, subsequent to stripping of the resist 30, an undamaged Oxide-Nitride-Silicon structure 38, 40, 42 as illustrated in Fig. 4B remains.

This remaining layered structure as illustrated in Fig. 4B is then subsequently processed in accordance with the present invention by oxidizing the silicon sub-layer 42 into a thermal oxide so as to arrive at a final ONO insulating layer 22 as required by the memory cell 12 of the illustrated embodiment. Also, the formation of the upper oxide layer at this stage can also assist with the formation of an appropriately thick high-voltage oxide for the peripheral transistor 14.

It should be appreciated that the important aspect of the present invention relates to the provision of an initial Oxide-Nitride-Silicon insulating layer structure which, subsequent to photoresist stripping, can then be readily altered to an ONO insulating layered structure by oxidation of the upper silicon sub-layer and so the invention is not restricted to the details of the particularly embodiment illustrated herein and relating to one particularly form of memory cell arrangement.

CLAIMS:

1. A method of forming a semiconductor structure comprising a substrate having a patterned ONO insulating layer over a portion thereof and characterized by the steps of forming an insulating layer comprising an Oxide-Nitride-Silicon layered structure on the substrate, applying a photoresist to the silicon surface as part of a patterning process and stripping the photoresist once a required patterning step has been completed, and subsequently re-oxidizing the silicon layer of the remaining Oxide-Nitride-Silicon structure so as to form an ONO insulating layer structure.

2. A method as claimed in claim 1, wherein the silicon layer comprises an amorphous silicon layer.

3. A method as claimed in claim 1 or 2, wherein a non-volatile memory cell is applied as part of the semiconductor structure, which non-volatile memory cell employs the ONO insulating layer between a floating gate and control gate thereof.

4. A method as claimed in claim 3, wherein the non-volatile memory cell is applied with a control gate formed from a conductive layer which also serves to form part of a peripheral semiconductor structure.

5. A method as claimed in claim 1, 2, 3 or 4, wherein the subsequent oxidation of the silicon sub-layer of the Oxide-Nitride-Silicon insulating layer is arranged also to provide a high voltage oxide layer for a peripheral structure.

6. A method as claimed in any one of claims 1 to 5, wherein the silicon layer is re-oxidized into a thermal oxide.

ABSTRACT:

(67)

The present invention provides for a method of forming a semiconductor structure (10) comprising a substrate (12) having a patterned Oxide-Nitride-Oxide (ONO) insulating layer (22) provided over a portion of the substrate (12). The invention employs an Oxide-Nitride-Silicon structure (38, 40, 42) as the basis for the ONO layer and which has the advantage that the upper silicon sub-layer (42) of the structure resists damage during the photoresist stripping step of a patterning process and is then available for re-oxidizing into a oxide layer forming the upper sub-layer of the required ONO structure.

Fig. 1

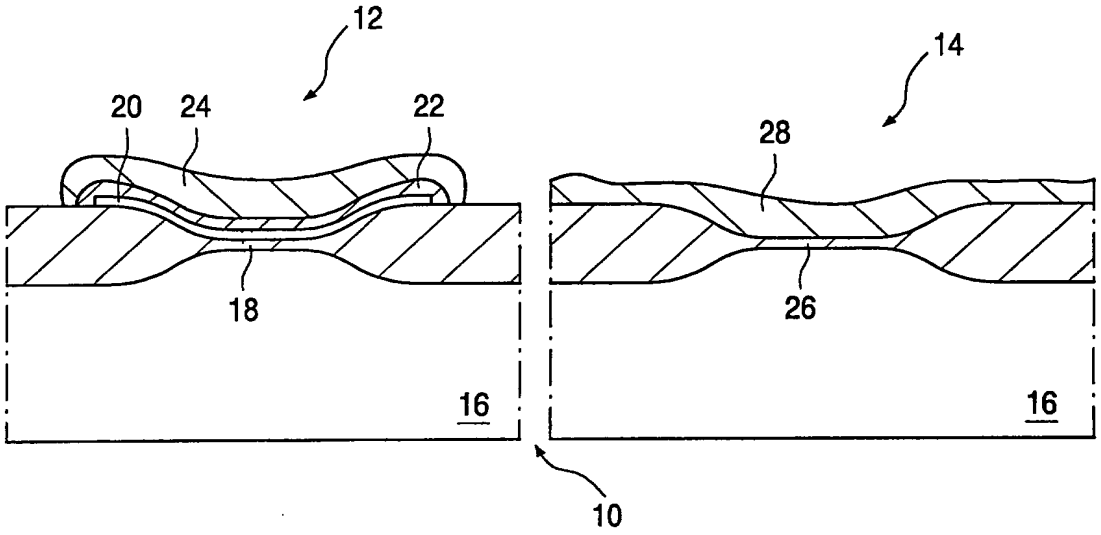

FIG. 1

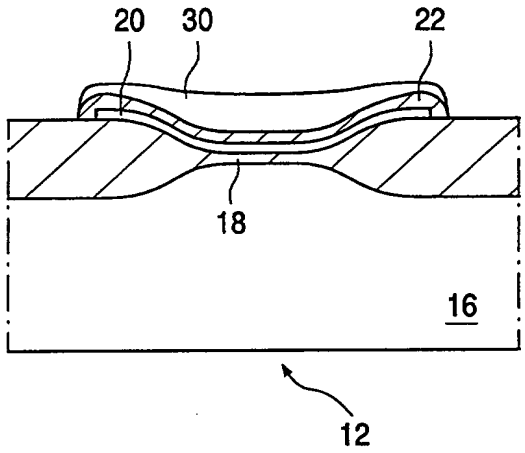

FIG. 2

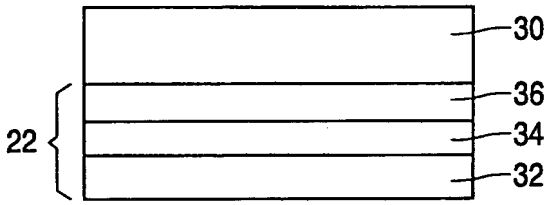

FIG. 3A

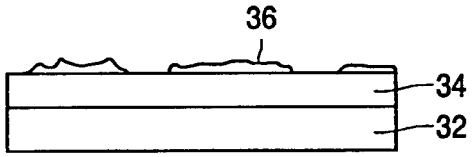

FIG. 3B

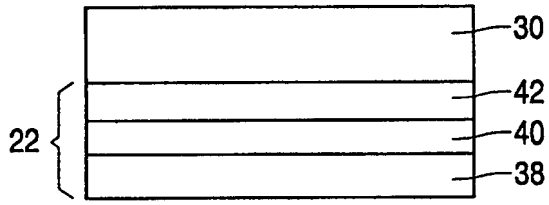

FIG. 4A

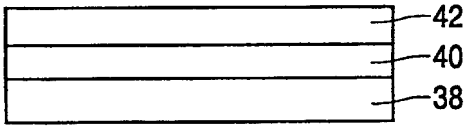

FIG. 4B